PVP 14

Code: CS2T4

I B.Tech - II Semester – Regular Examinations – April 2016

DIGITAL LOGIC DESIGN

(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) How many AND gates are required to realize Y = CD+EF+G.

b) The hexadecimal equivalent of $(1095)_{10}$ is

c) The process of entering data into a ROM is called

d) When the set of input data to an even parity generator is 0111, the output will be

e) The number 140 in octal is equivalent to _____ in decimal.

f) The output of SR flip flop when S=1, R=0 is

g) The 2's complement of the number 1101110 is

h) How many two input AND gates and two input OR gates are required to realize Y = BD+CE+AB

i) Convert the octal number 7401 to Binary.

j) Perform 2's complement subtraction of $(7)_{10}-(11)_{10}$.

k) What is the Gray equivalent of $(25)_{10}$

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2.

a) Perform the following arithmetic operations. 8 M

i. $(57)_{10}$ - $(81)_{10}$ using 2's compliment

ii. $(ABCDF)_{16} + (BFCDA)_{16}$

b) Convert the following. 8 M

i. $(10101111)_2 = (\quad)_8$

ii. $(7642.4)_8 = (\quad)_{10}$

iii. $(FCDF)_{16} = (\quad)_2$

iv. $(123.48)_{10} = (\quad)_2$

3.

a) Simplify the function F(A,B,C,D) = ∑m (0,2,6,11,12,13,14) using k-maps and implement the circuit using NAND gate only. 8 M

b) Simplify the function F(A,B,C,D) = ∑m (1,4,6,7,8,9,10,11,15) using Tabulation Method. 8 M

4.

a) Design a Full adder using Half adders and carry look ahead adders. 8 M

b) Design a BCD-to decimal decoder. 8 M

5.

a) Differentiate between PROM and RAM structures. 8 M

b) Which Memory device is fastest among RAMs, ROMs and CAMs? Justify. 8 M

6.

a) With the aid of external logic, convert D type flip-flop to a JK flip-flop. 8 M

b) Design a synchronous modulo-12 counter using NAND gates and JK flip flops . 8 M